AGILENT 307x In-Circuit Test Programming Standards

Revision 2.30
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1.0 Standard AGILENT 3070 ICT

ECT will develop the most comprehensive in-circuit test program possible within the capabilities of the Agilent 3070 board test system and the testability constraints of the card. ECT will perform all test program development, debug and fixture design. Our Programs are developed using Agilent’s 3070 board test system software and other proprietary software written by our consultants.

ECT will supply the customer with analog tests that reliably measure components using methods and limits established by Agilent’s In-circuit Program Generator (IPG). Our programs will provide reliable Digital and Mixed device tests with fault coverage specified by the client or dependent upon Agilent’s standard device libraries.¹

ECT offers six levels of custom test development for non-library devices.² The client can select any one of six test options for each non-library device. The standard test option offered by ECT for non-library devices is a combination of AGILENT VTEP/TestJet and a custom developed powered Presence and Orientation (P&O) test as outlined in sections 3.1, 3.2. The combination of a P&O test and AGILENT VTEP/TestJet® is a high fault coverage test solution for complex non-library devices. ECT recommends this solution to its clients that cannot justify the expense of developing a comprehensive custom library test such as ECT’s Enhanced or Basic I/O tests (outlined in section 3.4,3.5). For custom analog or mixed devices the client can provide test specifications, detailed data sheets or request AGILENT VTEP/TestJet®/P&O option. ECT will provide as standard an analog DC or frequency P&O measurement. ECT will work closely with the client to select the optimal test solution for each non-library device.

Devices that IPG evaluates as untestable due to topology constraints will have no test coverage. However, test coverage is usually possible using cluster, board level functional or silicon nail boundary scan testing. All such tests must be specified in the quotation. ECT often cannot predict that IPG will evaluate a device as untestable until the board test is developed. In such cases, ECT will provide a list of devices that are untestable and the client may request further test enhancements. In most cases additional compensation is required to enhance test coverage. ECT will work with the client to identify areas not covered by a standard IPG generated test. This insures the highest fault coverage is obtained on each in-circuit test. ECT quotations are based on a test plan that strives for maximum fault coverage. For example, when topology problems and testability is a concern for a particular device (that has a full library test) ECT will recommend using VTEP/TestJet in combination with the library test. VTEP/TestJet insures opens coverage on accessible pins and provides a backup or supplemental coverage. When considering quotes from other vendors be sure that they are offering the same level of analysis, test coverage, and service. Our quotations are always developed by Experienced Programmers not by sales personnel. All ICT programs are not created equal. Quality test programs are dependent upon the experience and knowledge of the programmers, at ECT: Advanced Programming is Guaranteed.

¹ ECT also has an extensive custom library.
² Each non-library device will be identified and listed with a suggested test option on each quotation supplied by ECT.
2.0 Non-Standard Test Development

The items below must be specifically requested by the customer, and included on the quotation.

1. Any digital device test that is not part of the current standard AGILENT 3070 library or ECT’s custom library requiring higher test coverage than VTEP/TestJet, and P&O test.
2. Any passive analog part test that cannot be described in the parts description editor.
3. Any active analog IC test that is not part of the standard AGILENT 3070 library or ECT’s custom library requiring higher test coverage than VTEP/TestJet and DC P&O test.
4. Digital cluster testing.
5. DriveThrough Testing (Digital Drive Through Series Termination Resistors)
6. Analog functional or cluster testing not specified in section 4.2.X.
7. Silicon nail boundary scan testing.
8. All Customer and third party tests that are not verified on the AGILENT 3070.
9. Backer gates and/or special fixturing requirements.
10. In-circuit device programming/re-programming.
12. ISP, Flash or EEprom Programing
3.0 Non-Library Device Test Options

Fault coverage is the percentage of non power/ground functional pins tested as a logic high and logic low that are probe accessible on the circuit board under test. The customer must supply ECT with complete device data sheets and functional specifications for these test options.

3.1 Setup Only Test
A Setup Only Test will embody no test vectors but will contain any disabling information so that surrounding devices can be properly tested. The test will also assure proper tester resource allocation to insure that a full pin test can be implemented at a later time without multiplexing conflicts in the fixture. The accuracy of each setup test will depend upon the quality and scope of device data supplied to ECT by the client.

3.2 Presence and Orientation (P&O) Test
A presence and orientation test will consist of all the features of a set up test (section 3.1). The purpose of the test is to verify the presence and orientation of the device. This test will verify at least one output as a logic high and a logic low or two or more outputs at a stable low. This test option in combination with AGILENT VTEP/TestJet is a high fault coverage test solution. The VTEP/TestJet detects solder opens and the Powered P&O checks the remainder of the fault spectrum by determining that the component is alive and is positioned correctly.

3.3 Minimum I/O Test
A Minimum I/O Test will consist of all the features of P&O test (section 3.2) and will test at least 20% of the pins. This test will be written to accommodate the configuration of the target device under test and may or may not be transportable to other circuits. This test will assure proper tester resource allocation.

3.4 Basic I/O Test
This test will include all of the features of the Minimum I/O test (section 3.3) but will provide pin test coverage of at least 80%. This test will be written to accommodate the configuration of the target device under test and may or may not be transportable to other circuits.

3.5 Enhanced I/O Test
This test will include all features of the Basic I/O test (section 3.4) but will cover 95-100% of non topology constrained pins. For simple I.C.’s all internal functional blocks will be exercised. For complex L.S.I. and V.L.S.I. devices, the internal functional blocks, modes, instructions, etc., will only be exercised as needed for the purpose of producing I/O activity. This test will be written to accommodate the configuration of the target device under test and may or may not be transportable to other circuits.
4.0 Standard Test Methods and Procedures

4.1 Shorts Testing
Shorts testing will be performed between all nodes except those that are inaccessible and not part of an interconnect boundary scan powered shorts test. Shorts testing will be done using the methods described in the "Analog and Shorts" manual for the AGILENT 3070 Board Test System. Upon failure the diagnostic output will report common devices and the net list. The diagnostic print out will not report “phantom shorts” unless requested by client. ECT has determined by experience that reporting “phantom shorts” does not improve failure ticket interpretation.

4.2 Analog Device Testing
All discrete analog devices that are recognized by IPG will be tested using 2,3,4 or 6 wire measurements as written by IPG. The customer must specify specific devices for mandatory 4 or 6 wire measurements. The customer may specify a Tolerance Multiplier (see the "Analog and Shorts" manual for the AGILENT 3070 Board Test System) to be used by IPG for the entire board or for specific parts. Unless stated otherwise by the client a tolerance multiplier of 3 will be used by IPG when generating analog tests.

CAPS
Unless specified by the customer the tolerances will be set to:
Minimum value will be 20%
10% will be set to 35%
20% will be set to 40%
+80/-20% will be set to +100/40%

RESISTORS
Unless specified by the customer the tolerances will be set to:
All pull up/down resistors less than 10% will be set to 10%
All small value series termination resistors (< 100 ohms) will be set to +20% -1%(or base tolerance) Resistors in critical “analog” type circuitry will be evaluated and set accordingly, typically these will be set at 5%.

4.2.1 Capacitors/Resistors in Parallel:
Capacitors/Resistors in parallel (such as bypass capacitors) are tested as one capacitor/resistor. Missing bypass capacitors are not detectable with in-circuit tests.
4.2.2 Passive Analog Device Packs:
Analog device packs such as resistors, capacitors, diodes etc. will have part description libraries written. Analog device packs that integrate multiple analog parts into one package will be considered non standard library devices if they cannot be described by the AGILENT 3070 parts description editor. AGILENT VTEP/TestJet® may be specified by the customer to test for solder opens on custom analog device packs.

4.2.3 Jumpers/Switches:
Jumpers/Switches will be tested in the open position unless otherwise noted on the schematic. In the event that a "normal" position is specified for a switch, it will be tested in that position, otherwise all switches will be tested as normally open.

4.2.4 Connectors:
ECT places probes directly on connectors as standard practice providing that board topology and probe density allows. This permits testing of internal traces from card edge to components. In some cases it is possible to detect a number of connector problems using this method. Alternatively, AGILENT VTEP/TestJet® is a high fault coverage solution. AGILENT VTEP/TestJet on connectors allows detection of solder opens on functional pins and can detect missing connectors. ECT will select surface mount connectors for VTEP/Testjet. The customer must specifically request the use of AGILENT VTEP/TestJet® on through-hole connectors. Another option is the use of switch probes to detect presence and/or orientation of connectors. If switch probes are preferred, the customer must specify which connectors to use switch probes and if the connector is polarized so that the switch probes is being implemented to detect orientation of the connector.

4.2.5 Potentiometers:
Potentiometers will have a test written that will require manual adjustment by the operator unless specified otherwise by the customer.

4.2.6 Variable Resistors:
Variable Resistors will be tested as a standard resistor, with a test for 1/2 of the nominal value. An interactive test will not be written unless otherwise specified by the customer.

4.2.7 Inductors/Coils/Chokes/Transformers:
Inductance measurements are taken if the device specification is between 25uH/100H. Ferrite Beads, small Inductors, Transformer windings etc. will be tested as Jumpers or Resistors unless specified by the customer. Circuit topology often limits accurate and stable inductance measurements.
4.2.8 **Diodes/Zeners:**
Diodes will be tested for forward bias voltage. Zener Diodes will be tested for reverse break down voltage up to 18V. If the Zener break down voltage exceeds 18V then Zener Diodes will be tested for forward voltage drop only. LEDs can be tested for the correct color using many different methods ranging from prompting the operator to verify the color to automated test methods. ECT will identify LEDs on the board and suggest, as a separate quote line-item, automated color testing.

4.2.9 **Bipolar Transistors:**
Bipolar Transistors are tested without power applied to the board. The base emitter diode junction and the base collector junction will be tested as standard diodes. IPG will generate a gain test that will not be debugged unless specified by the customer, and included in the quote.

4.2.10 **Field Effect Transistors:**
Field Effect Transistors will be tested on a "best effort" basis. IPG FET tests will not be used. Where circuit topology allows ECT uses a combination of Analog powered and diode measurements for full coverage. ECT FET tests proved excellent functional and manufacturing fault coverage. Most FET’s have a protection diode that will be modeled in a part library and measured un-powered. This tests the solder connection of the Drain and Source. A Powered “On” test will verify the GATE connection and that the device can be turned on.

4.2.11 **Relay Contacts/Relay Coils:**
Relay Coils will be tested as resistors or jumpers depending upon the magnitude of the coil resistance. Relay contacts will be tested with digital/analog or mixed techniques depending upon circuit topology and other constraints.

4.2.12 **Operational Amplifiers:**
Operational Amplifiers and voltage comparitors will be tested to insure that outputs reach rail voltages. Gain testing or other specific measurements on operational amplifiers is considered custom test development.

4.2.13 **Voltage Regulators:**
Voltage Regulators and Sources will be tested for proper output. Limits will be $\pm 10\%$ unless specified otherwise. Often voltage sources must be tested as functional clusters, and diagnosis of specific devices within the functional cluster is not possible.

4.3 **Digital Integrated Circuit Testing**
Fault coverage of the unit under test (UUT) depends on several important factors:

- The testability of the target design.
- The probe accessibility of nets on the PC board.
- The availability of comprehensive I.C. data sheets.
- The capability and configuration of the AGILENT 3070 Board Test System.
- The quality of the libraries used by IPG.

Disabling methods must be supplied for every digital UUT on the circuit board attached to "bussed nodes" (nodes with more than one device output attached). These disable methods may come from the standard library tests. However, for boards with non-library custom digital parts, the customer must supply disable methods for these devices. ECT will not be responsible for the repeatability of any digital tests attached to non-disabled devices. Back-driving is not an alternative for large bused devices because of potential oscillation and component damage.

4.3.1 Random Access Memory (RAM):
RAM will be tested using an ECT’s standard memory test algorithm. This algorithm verifies that all data and address bus pins are soldered correctly. A full cell check is not implemented unless the customer specifies. Full cell memory tests are not required to detect common manufacturing problems such as stuck at pins. ECT recommends placing VTEP/TestJet on all memory devices as a supplemental/backup test especially on J-lead parts. DDRII and newer devices require communication speeds greater than those possible at ICT and will therefore only have VTEP/TestJet coverage.

4.3.2 EPROMs and PROMs:
EPROMs/PROMs are tested using CRC techniques as described in the "Digital Test Methods" AGILENT 3070 Board Test System manual. CRC signatures are learned from the devices supplied at the time a known good board is tested after program debug.

4.3.3 Programmable Logic Devices:
Programmable Logic Devices such as PALs are tested with vectors generated from customer supplied JEDEC files. All non-boundary scan PLDs are considered custom tests and must be included in the quote. FPGAs and PLDs having boundary scan (i.e. Xilinx 4000 some AMD MACH, etc.) will have standard boundary scan tests as out lined in section 5.0. Standard test methods for larger programmable logic devices is VTEP/TestJet and full resource setup test. ECT recommends placing VTEP/TestJet on all PAL's FPGA's and PLD's as a supplemental/backup test.

4.3.3 EEPROMs and Flash Ram In-Circuit Programming:
EEPROMs and Flash Ram may be programmed or re-programmed in-circuit. The customer needs to supply the appropriate data files and all upstream devices must have disable methods. All in-circuit device programming is non-standard and must be specified in the quotation. When Flash devices are not being programmed in-circuit programming pins cannot be tested by the library. Therefore ECT recommends placing
VTEP/TestJet on all FLASH devices to provide opens coverage on programming pins (such as Write Enable).

4.4 **AGILENT VTEP/TestJet ®**

For devices that use AGILENT VTEP/TestJet, ECT will adjust the threshold calculated by IPG to a tighter tolerance on several pins. This fine adjustment will enable the VTEP/TestJet to detect a missing component in addition to detecting solder opens. ECT has determined through experience that IPG generated thresholds are sometimes sufficiently high to pass a device that is completely missing from the board. AGILENT VTEP/TestJet cannot detect opens on fixed pins such as VCC and Ground or certain topological conditions such as pins tied directly to capacitors. Topological limitations are not always apparent until after debug is attempted. Therefore, all VTEP/TestJet testing implemented by ECT is dependent upon the limitations of the tester, device type and circuit topology. ECT cannot guarantee that all devices specified for AGILENT VTEP/TestJet will be repeatable or the package type will be suitable for testing.

4.4.1 **VTEP-NPM Modeling:**

VTEP-NPM Modeling from AGILENT allows for power and ground pins on connectors to be tested using VTEP, if the power or ground pin on the connector is surrounded by signal pins and a SPICE model exists for the connector. If an NPM model does not exist, but a SPICE model does, a request can be made to AGILENT to create the NPM model.

4.4.2 **VTEP-CET:**

CET or Cover-Extend is the latest VTEP enhancement from AGILENT. CET allows for VTEP testing of ICs connected to Boundary Scan parts without physical access. The Boundary Scan part must have a valid BSDL file along with the internal Scan cell structure to drive signals to the IC to be tested. CET requires 7.20pd software, the CET upgrade kit from AGILENT, and a software license in order to take advantage of these new features. ECT has practical experience with both the CET hardware and software and can debug CET tests in our facility.

4.5 **AGILENT Polarity Check ®**

Polarized capacitors such as tantalum and electrolytic can be tested using AGILENT Polarity Check. ECT recommends placing Polarity Check on all polarized capacitors because of the increased fault coverage obtained. However, certain topological configurations and device types are not testable due to low board impedance or shielded package design. It is often impossible to predict these problems until the tests are developed or debugged. ECT cannot guarantee that all devices specified for polarity check will be repeatable or suitable testing.
5.0 IEEE-1149.1 AND 1149.6 BOUNDARY SCAN TESTING

5.1 Single Device Boundary Scan Test
Any devices that are IEEE-1149.1 compliant and have BSDL (Boundary Scan Description Language) files will have parallel toggle tests developed by ECT. If conditions stated in section 4.3 are applicable then a parallel toggle test will provide the coverage of an Enhanced I/O test as described in section 3.5 (with the exception that no internal logic is exercised).

5.2 ECT’s On-line Boundary Scan Diagnostics Option
ECT can provide the client with on-line or off-line diagnostics to help isolate manufacturing faults to the pin level on failing boundary scan devices. Automatic on-line diagnostics developed by ECT are used by customers that do not have Interconnect Plus capability. Our diagnostics give the same device pin diagnostic resolution offered by Interconnect Plus at a fraction of the cost. Our on-line diagnostics report the actual pins that are failing. Normal AGILENT 3070 diagnostics only report the scan out pin (TDO) for all input or bi-directional pin failures. On-line or off-line diagnostics must be requested by the client and included in the quotation from ECT.

IEEE-1149.1 Boundary Scan Device Internal Structure
5.3 **Multiple Device Interconnect Plus Boundary Scan Testing**

Client must have purchased the Advanced Boundary Scan software option from Agilent for boundary scan interconnect testing. All tests and diagnostics will be developed by IPG. The quality of the test and fault coverage will be determined by the testability, accessibility and conditions outlined in section 4.3. The standard tests will be supplied if the boundary scan chain is connected to comply with the IEEE-1149.1 standard. Additional interconnect testing other than that developed by IPG is considered custom engineering and must be specified by the customer, and stated in the quote from ECT.

5.4 **Silicon Nail Boundary Scan Testing**

ECT can develop custom silicon nail tests using boundary scan devices and regular fixture probes to test inaccessible digital devices. All silicon nail tests are custom tests developed by ECT. Silicon nail tests and custom boundary scan cluster tests must be requested by client and stated in the quote from ECT. Because of fault aliasing issues arising from the silicon nail testing all diagnostics will be heuristic.

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**ECT Closed Loop Scan® Process**

*Advanced Programming Guaranteed*

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5.5 **1149.6 Advanced I/O Boundary Scan Testing**

The IEEE 1149.6 Standard was approved in March 2003 to extend the capabilities of the 1149.1 standard to include AC-coupled and/or differential nets. As serial bus speeds increased the standard DC coupled signals were not longer sufficient to carry the signals at the speeds necessary for more advanced communications. Also, the standard Boundary Scan cell was not designed for this type of communication. Using the new 1149.6 Boundary Scan license from AGILENT allows for the testing of ICs whose Boundary Scan architecture implements this new feature. ECT has purchased this software license and has implemented the 1149.6 Advanced I/O Boundary Scan testing on several applications. ECT has also designed and implemented loop-back modules for testing AC-coupled signals that travel from 1149.6 compliant parts to connectors and then off the board. By looping these signals back to the device more complete coverage can be obtained.

6.0 **OTHER/MIXED INTEGRATED CIRCUIT TESTING**
Mixed analog and digital devices such as AD and DA converters will have standard “best effort” analog DC and digital P&O measurements combined with AGILENT VTEP/TestJet. Excellent test coverage for mixed devices is obtained by using this combination. ECT uses this method as standard because it offers the customer high fault coverage at low cost. Alternatively, ECT can develop a complete mixed in-circuit library test. The digital portion of the device test is specified by selecting one of the six digital library options outlined in section 3.0. The analog portion of the test is developed to customer specifications or data sheets. Testing will be limited to the capability of the Agilent 3070 board test system, circuit topology and node accessibility. Accurate and complete data sheets are necessary for all mixed test options. Mixed library tests other than the VTEP/TestJet/P&O combination must be requested by the customer and include in the quotation from ECT.

7.0 ANALOG-ONLY IN-CIRCUIT TESTING

ECT has also developed a reduced cost fixture and program for testing of PCBs normally tested on a flying-probe machine. The Analog-Only option allows for quicker testing of boards versus the test time of the flying probe machine. A fixture and program are developed targeting an unpowered tester configuration to allow for shorter development cycles and faster turn times. Analog-Only fixtures can help reduce the backup of products waiting to be tested on a flying probe machine.
8.0 TEST FIXTURE

ECT will design and build a fixture for the Agilent 3070 Board Test System to be used in conjunction with the test program.

8.1 Test Fixture Quotations

Quotations issued for fixtures before the completion of a test program must be considered budgetary. ECT is not responsible for price increases due to unforeseen additional resource requirements. ECT will advise the client in writing as soon as any additional fixturing requirements are found.
9.0 CUSTOMER SUPPLIED MATERIALS & DOCUMENTATION

The Customer must supply the materials and documentation listed below:

**For a Quotation:**
- CAD Files – current rev
- Schematics – current rev
- Testhead Configuration File
- Programming Statement of Work – If none exists, ECT will use this programming standards document as a basis for the quotation
- Special, non-standard test requests (See 2.0 Non-Standard Test Development)

**For a Total Solution Project, in addition to the items listed above:**
- AVL-Bill of Materials that included manufacturer name, part number, and reference designator (current revision)
- Gerber Files (minimum of outside layers – solder masks, silkscreens, and drill)
- Data sheets/BSDLs for all custom/non-library IC’s (if not available over the internet).
- Disabling information for all custom non-library devices and programmable logic.
- Autofile number.
- Loaded Printed Circuit Board, mechanically accurate to current rev (For fixture design)
- Known Good Loaded Printed Circuit Board (KGB), I minimum, 2 to three preferred (For Test Program Debug and Validation)
- Bare PC board (optional).

Quotations will normally be issued by ECT after all the data and materials necessary for the project have been received and all custom work is identified. Any changes to the data, materials or test levels after the quote has been issued may require a quote update. Engineering Change Orders, (E.C.O’s.), that occur once work has commenced on a test program will require additional compensation for ECT to implement the E.C.O’s.

All material received must be of the same revision level. The test program and fixture will be for only the revision level supplied unless otherwise specified in the quotation. Delivery dates are calculated from the receipt of the last piece of material or documentation. Programs/Tests cannot be guaranteed if the program is not debugged on a known good board.

ECT is not responsible for the loss of test coverage due to errors in customer supplied CAD data. Ultimately, the quality of the test delivered by ECT will depend on the accuracy of the data describing the circuit board to be tested.

Tests developed by the client, or third parties other than Agilent can be utilized by ECT where appropriate. However, tests that have not been debugged or verified on an AGILENT 3070 must be identified as such so that debug time can be considered during the formulation of a quote. Coverage and/or reliability of user and third party tests cannot be guaranteed by ECT.
10.0 DELIVERABLES

10.1 Test Program Files
Test program files loaded into 1 DAT tapes or CD. These files include all the Custom Libraries, Fixture Files, Documentation on Fixture Electronics and all the necessary files needed to run, sustain, or regenerate the test program.

10.2 Test Coverage and Quality Reports
ECT provides a test coverage report based on ECT format. The reports also list the untested or limited test components. ECT runs Agilent Board Grader. All the reports can be found in the “bdg_data” directory.

11.0 ACCEPTANCE CRITERIA

This document provides the criteria for determining that ECT has fulfilled its obligations to supply an Agilent3070 ICT Test Program for testing the specified board intended on an Agilent3070 system with the requirements mentioned in this document. It specifies a procedure by which ECT will demonstrate that the program fulfills the agreed test functions as specified in this SOW have been successfully implemented.

11.1 Acceptance Test Environment

Tester : Customer shall provide the tester hardware during Acceptance process. The tester must pass “Full Diagnostic” without any errors.

Boards : Customer shall provide ten pieces of known good board (KGB).

11.1 Acceptance Test Procedure
ECT engineer together with customer shall execute the Acceptance Procedure as specified in the Acceptance Checklist. Each step shall be checked off when observed results are as specified in the Acceptance Checklist.

The Acceptance process will be considered successfully completed when all steps have been checked off. At that time, the Acceptance Checklist will be signed by the appropriate parties.

12.0 WARRANTY

12.1 Program
The Test Program is on warranty for a period of ninety (90) days following the date of acceptance of work (Acceptance Checklist). The warranty covers any gaps in deliverables between the test program delivered and the SOW. Customer must notify ECT in writing of any such gaps. ECT will make its best effort to resolve the gaps in a timely manner.
All program generated by ECT will be archived for a period of one years from invoice of the project. Customer should maintain their own backup periodically. Customer will not be notified prior to destruction of project data or files after one year.

12.1 Fixture

The fixture is guaranteed free from workmanship and material defects for ninety (90) days after acceptance by Customer. Test failures due to Engineer-Change-Order (ECO) or component vendor change are not included in the warranty.

13.0 NON-DISCLOSURE AGREEMENTS

ECT conducts business to the highest of ethical standards. ECT will enter into legally binding non-disclosure agreements with it’s customers to protect proprietary information. Non-disclosure agreements are returned to clients promptly by FAX, signed and scanned, and hard copies are returned by mail or Federal Express.