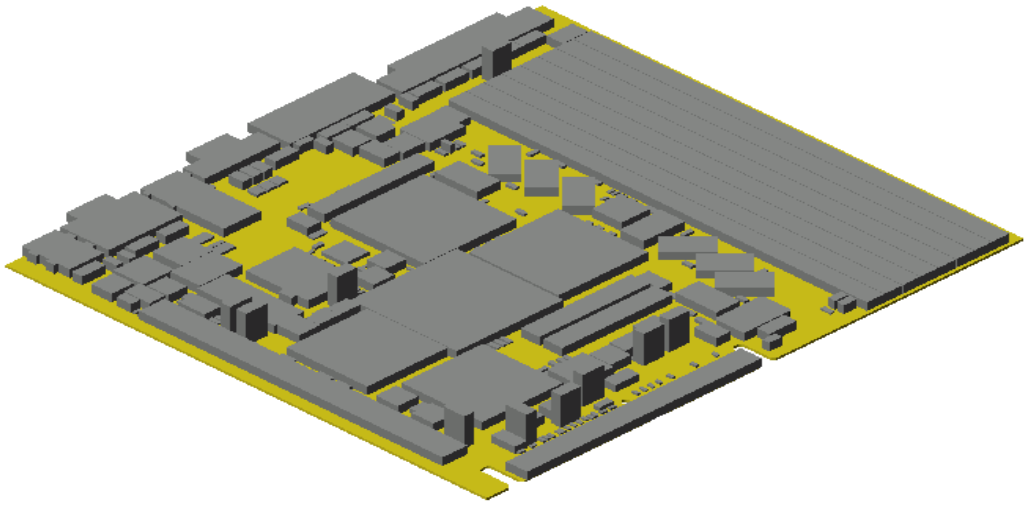
EVERETT CHARLES TECHNOLOGIES

Automated Zero-Flex
File Requirements



CAD File Formatting Instructions

The list of Electrical CAD Systems currently supported by the Automated Zero-Flex Fixturing process is as follows:

1. Protel Products:
   - Accel EDA
   - PCAD 2000
   - Tango
   - Protel Design
   - PCAD Design

2. Cadence Products:
   - Allegro
   - Orcad Layout Plus

3. Mentor Graphics Products:
   - Boardstation
   - Neutral
   - Veribest

4. INNOVEDA Products:
   - Pads PCB
   - Pads Pro
   - Pads 2000

5. Intercept Products:
   - SciCards
   - Harris EDA
   - Encore PCB

6. Zuken-Redac Products:
   - Zuken-Redac PWS
   - Zuken-Redac Board Designer
   - Incases Theda

7. Industry Standard GenCAM files

Detailed formatting instructions for each Electrical CAD system are provided on the following pages.

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1. Protel Products

a. Accel EDA, PCAD 2000, Tango Pro

- File Used for Automated Zero-Flex Fixturing processing: .PCB (ASCII)
- How to Produce File: Standard file save in ASCII format.
- Systems: Accel EDA v.14 and v.15, Tango Pro v.12 & 13 and PCAD 2000 (.pcb).

b. PCAD Design

- File Used for Automated Zero-Flex Fixturing processing: .PDF
- System Supported: PCAD (DOS based) 2.X through 8.X., (.pdf)
- How to Produce files: Use command sequence ***PDIFOUT -I pcb_file***, where pcb_file is the PCAD .PCB file (Binary Database)

c. Protel PCB

- System Supported: Protel for Windows PCB versions 2.7, 2.8, 3, 4, and Protel 99.
- How to produce files:

  i. Before creating your ASCII file in Protel, you should run the net connections by going to Auto Route | Connection.
  ii. When that finishes select the command FILE MENU | EXPORT.
  iii. Select the TEXT Option "Protel PCB 2.8 ASCII File (*.PCB)".
  iv. Name the File then click SAVE.

  Notes:

  - In Protel 98, select the version 2.8 TEXT export option
  - In Protel version 3, select the version 2.8 TEXT export option
  - In Protel version 4, select the version 2.8 TEXT export option

2. Cadence Design Systems

a. Allegro

- Files Used for Automated Zero-Flex Fixturing processing: brd.txt, pad.txt, rte.txt, sym.txt
- Systems Supported: Cadence Allegro PCB Layout versions 5 through current under UNIX & 12.2 through current under Windows NT.

- How to Produce Files:

  Note: The Allegro extract utility requires an extract script (valext.txt) which will be provided by ECT-Engineering on request.

  i. From the UNIX command prompt type the following to execute the extract utility:

     extract *<return>*

  ii. Enter the following as prompted:
     - Layout name (*.brd): *path/filename* <return>
     - Extract command file (*.txt): *path*/***valext*** <return>
     - Extract output filename (*.txt): *path*/***brd*** <return>
     - Additional output filename (<return> if none) (*.txt): *path*/***pad*** <return>
     - Additional output filename (<return> if none) (*.txt): *path*/***sym*** <return>
     - Additional output filename (<return> if none) (*.txt): *path*/***rte*** <return>
       - Additional output filename (<return> if none) (*.txt): <return>

  iii. This creates the for files for use in creating the Automated Zero-Flex Fixturing file: brd.txt, pad.txt, sym.txt, rte.txt

b. <u>Orcad Layout Plus</u>

- File Used for Automated Zero-Flex Fixturing processing: .MIN
- System Supported: OrCAD Layout Plus version 7.x through version 9.x
- How to Produce file:

  i. Launch OrCAD Layout Plus.
  ii. From the initial screen select File | Export | MIN Interchange from the menu.
  iii. You will now be prompted to browse to and select the *.MAX (binary design) file for which you wish to generate a *.MIN file for. Browse to the desired file, select it, and click Open.
  iv. You will now be prompted to browse to a directory and provide a name for the .MIN file to be written. Browse to a directory, provide a file name, and click Save. You will now be prompted with an "Options" dialog. Select the All of the Above option and click OK to proceed.

v. OrCAD will now read the binary database and produce the MIN file.

3. Mentor Graphics

a. Boardstation

- Files Used for Automated Zero-Flex Fixturing processing: .prt, .cmp, .wir, .net, .lyr, .tec
- System Supported: Mentor Graphics (Boardstation) v8.x and higher on all platforms
- How to Produce files:

Note: Only the geom_ascii file needs to be saved in a special way, the other five files are in the standard Mentor format.

i. Launch LIBRARIAN.
ii. In the "Invoking LIBRARIAN" dialog select On a Design as your option.
iii. Select the design container to open in LIBRARIAN and press OK.
iv. In the "Invoking LIBRARIAN: Specify Technology" dialog select Standard PCB and press OK to proceed.
v. In the next dialog, "Invoking LIBRARIAN: Specify Switch", select the appropriate switches and click OK to proceed.
vi. Once LIBRARIAN has opened and the design library is loaded select File | Save | Save ASCII Geometries.
vii. Be sure to select the proper options to save all parts into a single ASCII file. The file generated will be given the name geom_ascii

b. Mentor Neutral File

- File Used for Automated Zero-Flex Fixturing processing: .NEU
- System Supported: Mentor Version 8.x.
- How to Produce files: Standard neutral file output.

c. VeriBest 99 and Later (.hkp):

- Files used for Automated Zero-Flex Fixturing processing: VB ASCII

i. Export VBASCII after the desired design has been loaded. From the menu select “File | Export | VB ASCII”.
ii. At the “Export VB ASCII” dialog the user will be prompted for a

directory to which to extract the VB ASCII files to and is given a list of optional files to export. All options should be selected and click "OK". The resulting files will be in the selected directory and will all have the .HKP extension.

d. <u>VeriBest 98 and prior:</u>

- Files used for Automated Zero-Flex Fixturing processing: See Below

i. Requires executable (vb2rsi.exe) which will be provided by ECT-Engineering on request.

ii. This is the minimum set of VeriBest PCB database files that must exist:

config.cbf	VeriBest PCB Configuration File
attached pin table	Pin Table
attached pad table	Pad Table
design.vbd	VeriBest PCB Design File
local2d.caf	Cell Library Data File
local2d.ccl	Cell Library File
netnames.cbf	Net Names File
schdb.cbf	Schematic Database
schnet.cbf	VBPCB Schematic Netlist
vbpcb.cpj	VBPCB Project File

Note: Make sure that the VeriBest PCB Pin and Pad Tables attached in Job Parameters are contained locally.

iii. **Execution:** Run "vb2rsi.exe" from the VeriBest PCB database directory.

iv. **Output:**

The following files are created and used for Automated Zero-Flex Fixturing processing:

eifo_cor.txt	- EIF Correspondence file
eifo_tec.txt	- Job Parameters Technology file
eifo_pad.txt	- Pad Table file
eifo_pin.txt	- Pin Table file
eifo_cel.txt	- Cell Library file
eifo_des.txt	- VeriBest PCB Design File (design.vbd)
eifo_clr.txt	- Job Parameters Clearances file

eifo_trn.txt - EIF Out Translator log file

4. INNOVEDA Products (PADS PCB, PADS PRO, PADS 2000)

- File Used for Automated Zero-Flex Fixturing processing: .ASC
- System Supported: all versions

5. Intercept Products (Scicards / Harris-EDA / Encore PCB)

- File Used for Automated Zero-Flex Fixturing processing: .DAT (CII File)
- System Supported: Scicards/Harris-EDA/Encore PCB CII versions 2 through 8
- How to Produce file:

  i. Load the CII (.DAT) file data into Scicards with the following command sequence: RULES for Technology ; NEWSHAPES for Shapes ; CADINTF input for Design
  ii. Export the file using the following command sequence EXPORT ; READABLE (REA00x) ; ALL OPTIONS ON.
  iii. Create the .DAT (CII File).

6. Zuken-Redac Products

a. Zuken-Redac PWS

- File Used for Automated Zero-Flex Fixturing processing: .BSF, .UDF, .MDF, .WDF, .WSF, .CCF, .PMA
- System Supported: CR3000
- How to Produce Files:

  ECT-Engineering will supply a batch file (READZUKN.txt) which must be run to extract the data needed. It is an ASCII file that must be ported to the system on which the Zuken software resides. Upon execution of READZUKN various Zuken binary files will be read and processed through Zuken decompilers. The result will be a series of ASCII files which are utilized for Automated Zero-Flex Fixturing processing.

b. Zuken-Redac Board Designer

- File Used for Automated Zero-Flex Fixturing processing: . .FTF and .PCF files generated with Board Designer decompile utilities.

- System Supported: CR5000

c. CADStar for Windows/Visula

- File Used for Automated Zero-Flex Fixturing processing: CADIF .PAF file
- Systems Supported: CADStar for Windows and Visula, latest releases.
- How to Produce file:

  CADStar for Windows:

  1. In CADStar, go to the File Menu and select Export.
  2. Select Format = Cadif.
  3. Click OK

  Visula:
  1. Load the board file into Visula
  2. Go to the Job menu and select Job | input/output | Neutral Archive | Output

d. Incases/Theda

- File Used for Automated Zero-Flex Fixturing processing: .TL
- System Supported: Version 2 to 4.x
- How to Produce file: Use ***board save TL*** command sequence to generate file(s).

7. GenCad

- The Automated Zero-Flex Fixturing process reads GenRad GenCAD files.
- Version Supported: v1.0 – v1.4

8. Industry Standard (GenCAM files)

- The Automated Zero-Flex Fixturing process also directly reads Industry Standard GenCAM files.
- Version Supported: v1.5